Amendments to the Claims:

The listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) An apparatus which detects a frame synchronization signal from a digital data signal reproduced from an optical disc, the apparatus comprising:

a synchronization signal detector, which detects and outputs a synchronization signal from the digital data signal;

a main frame synchronization signal generator, which detects and outputs a first valid synchronization signal from the synchronization signal as an internal frame synchronization signal, and generates and outputs a first insertion synchronization signal as the internal frame synchronization signal, if the first valid synchronization signal is not detected during a predetermined first time period;

a sub frame synchronization signal generator, which detects and outputs a second valid synchronization signal from the synchronization signal while the main frame synchronization signal generator generates the first insertion synchronization signal; and

a first output unit, which outputs a frame synchronization signal in response to the internal frame synchronization signal and the second valid synchronization signal, wherein the main frame synchronization signal generator stops generating the first insertion synchronization signal in response to the second valid synchronization signal, and detects and outputs the first valid synchronization signal as the internal frame synchronization signal.

2. (Currently Amended) The apparatus of claim 1, wherein the main frame synchronization signal generator comprises:

a first valid synchronization signal detector, which detects and outputs the first valid synchronization signal from the synchronization signal in response to a predetermined first window signal;

an ~~interval~~internal frame synchronization signal output unit, which outputs the internal frame synchronization signal in response to the first valid synchronization signal, the second valid synchronization signal, and the first insertion synchronization signal;

a first counter, which is reset in response to the internal frame synchronization signal, counts a predetermined channel clock signal, increases a count value, and outputs a first counting signal when the count value reaches a predetermined value;

a first window signal generator, which enables the first window signal during a predetermined second time period in response to the first counting signal; and

a first insertion synchronization signal generator, which generates the first insertion synchronization signal, if the first valid synchronization signal received from the first valid synchronization signal detector is not activated during the predetermined first time period.

3. (Original) The apparatus of claim 2, wherein the sub frame synchronization signal generator comprises:

a second valid synchronization signal detector, which detects and outputs the second valid synchronization signal from the synchronization signal in response to a predetermined second window signal;

a reset signal output unit, which outputs a reset signal in response to the synchronization signal and a second insertion synchronization signal;

a second counter, which is reset in response to the reset signal, counts a predetermined channel clock signal, increases a count value, and outputs a second counting signal when the count value reaches the predetermined value;

a second window signal generator, which enables the second window signal during the predetermined second time period in response to the second counting signal; and

a second insertion synchronization signal generator, which generates the second insertion synchronization signal if the synchronization signal received from the synchronization signal detector is not activated during the predetermined first time period after the second counter is reset.

4. (Original) The apparatus of claim 3, wherein the predetermined first time period is a time taken until the accumulated counting value reaches the predetermined value, after the first and the second counters are reset.

5. (Original) A method of detecting a frame synchronization signal in a frame synchronization signal detection apparatus of an optical disc system, the frame synchronization signal detection apparatus comprising: a synchronization signal detector which detects a synchronization signal from a digital data signal; a main frame synchronization signal generator, which outputs, as an internal frame synchronization signal, one of a first valid synchronization signal detected from the synchronization signal and an insertion synchronization signal internally generated; a sub frame synchronization signal generator, which detects a second valid synchronization signal, while the main frame synchronization signal generator generates the insertion synchronization signal; and an output unit, which outputs a frame synchronization signal, in response to the internal frame synchronization signal and the second valid synchronization signal, the method comprising:

(a) detecting the first valid synchronization signal from the digital data signal;

(b) outputting the first valid synchronization signal as the frame synchronization signal, when the first valid synchronization signal is detected within a predetermined time interval;

(c) generating and outputting the insertion synchronization signal as the frame synchronization signal, if the first valid synchronization signal is not detected during the predetermined time interval; and

(d) returning to step (a), if the second valid synchronization signal is activated while the insertion synchronization signal is generated.

6. (Original) The method of claim 5, wherein step (d) comprises:

(e) resetting a counter of the sub frame synchronization signal generator, when the synchronization signal is detected;

(f) the counter counting the channel clock signal;

(g) outputting the second valid synchronization signal as the frame synchronization signal if the second valid synchronization signal is detected when the count value of the counter reaches a predetermined value; and

(h) resetting the counter and returning to step (f), if the second valid synchronization signal is not detected when the count value of the counter reaches the predetermined value.